AMENDMENTS TO THE CLAIMS

The following listing of claims replaces all prior listings, and all prior versions, of claims in the application.

LISTING OF CLAIMS:

1. (Currently amended) A ~~recording format for information data in a~~ magnetic recording/reproduction apparatus, including a recording medium to which an information is recorded to a data sector by a predetermined format, and a magnetic head for recording/reproducing the information, comprising~~wherein~~:

a recording/reproducing signal processing circuit for processing the information to be recorded or reproduced;

said format on the medium comprising:

~~a recording code sequence format recorded on a recording medium comprises;~~

a preamble including additional information for the control of recorded position information, amplitude gain control and data timing recovery;

an information code composed of plural code sequence blocks; ~~including second redundant code bits (second parity code bits); and~~

a first redundant code composed of plural code sequence blocks ~~first redundant code bits for~~ used for hard-decision type data error correction; ~~(first parity code bits); and~~

a second redundant code inserted in the code sequence block used for soft output type error correction;

wherein the ~~length (number of code symbols) of each code block including redundant code bits in~~ number of code symbols of the second redundant code is

equal to or ~~shorter~~ less than a number of code ~~symbol units correctable by~~ symbols of the first redundant code ~~bits~~.

2. (Currently amended) The magnetic recording/reproducing apparatus ~~A recording format for information data~~ according to claim 1, wherein:

said first redundant code is a Reed-Solomon code, and

said second redundant code is a Turbo code~~the second redundant code bits (the parity code bits) are collectively recorded in predetermined positions in each code block~~.

3. (Currently amended) A recording/reproducing signal processing circuit including a recording signal processing system and a reproducing signal processing system, which is utilized for a storage recording/reproducing that reproduces an information code sequence consisting of a plurality of code bits recorded by a predetermined unit in a recording medium, ~~An information recording/reproducing encoding circuit provided with an error correction encoding circuit that applies coding for correcting code errors caused when an information code sequence is reproduced from an information recording medium to the information code sequence recorded onto the information recording medium,~~ said recording signal processing system comprising:

a first encoding circuit that applies first error-correction coding to the information code sequence by the predetermined unit, and adds a first redundant code sequence to said coded information code sequence, thereby generates an error-correction code sequence~~a unit of an input information code sequence (an information data sector) once recorded on the information recording medium in units~~

~~of predetermined code (code symbol) and executes the first error-correction coding for correcting the error code symbols equal or smaller than a predetermined number of code symbols, which are caused in the corresponding reproduced sector;~~

~~a circuit that adds a redundant code sequence by the first error-correction coding to the information data sector hereby output;~~

a concatenated encoder that:

divides the ~~contents of code sequence of the information data sector~~ error-correction code sequence output from the first encoding circuit ~~(that executes the first error-correction coding)~~ into continuous plural code sequence blocks having predetermined length, ~~and holds them;~~

stores the plural code sequence blocks,

executes

~~a second encoding circuit that executes~~ second error-correction coding for each code sequence block, and

generates a second redundant code sequence with referring to the contents of each code sequence block ~~held in the said circuit~~; and

a code switch that outputs the plural code sequence blocks and the second redundant code sequence alternatively, thereby generating the information code sequence comprised of the plural code sequence blocks;

wherein said information code sequence includes the first redundant code having a length of the code sequence block, the second redundant code is inserted in the code sequence block.

~~an error-correction encoding circuit that outputs a series of code sequence block as a code sequence recorded on the information recording medium after redundant code bits output from the second encoding circuit are inserted into the~~

~~corresponding code sequence block, wherein the length of the code sequence block in units of code symbol is set to a length equal or shorter than the number of code symbols correctable by the first error-correction coding, wherein:~~

~~after a code sequence corresponding to information code sequence recorded on an information recording medium is converted by the error-correction encoding circuit, it is output from the encoding circuit.~~

4. (Currently amended) The recording/reproducing signal processing circuit ~~An information recording/reproducing encoding circuit~~ according to claim 3, wherein said concatenated encoder comprises:

~~the encoding circuit that executes the second error-correction coding comprises:~~

a code permutation circuit ~~for processing a code sequence corresponding to the code sequence block in units of code length equal to the code sequence block;~~ that divides the error-correction code sequence output from the first encoding circuit into continuous plural code sequence blocks having predetermined lengths, and stores the plural code sequence blocks;

a second encoding circuit that executes second error-correction coding for each code sequence block, and generates a second redundant code sequence, referring to the contents of each code sequence block stored in the code permutation circuit.

~~memory circuits for holding the result of the code permutation in units of code length equal to the code sequence block;~~

~~encoding circuits that respectively executes predetermined second error-correction coding, referring to the contents of the memory circuits; and~~

~~circuit means that inserts redundant bits output by respective encoding circuits in a predetermined positions in the corresponding code sequence block held in the memory circuit beforehand.~~

5. (Currently amended) The recording/reproducing signal processing circuit ~~An information recording/reproducing encoding circuit~~ according to claim 4, said recording/reproducing signal processing system comprising:

a maximum-likelihood detector ~~soft-output decoder~~ that receives a reproduced signal sequence supplied from the recording medium and outputs the soft-output code information sequence, which is multi-valued information corresponding to a reliability code bit;~~information of each code bit to detect and correct code errors by the second error correction coding, wherein:~~

a multiplexer that divides the soft-output code information sequence into a first soft-output code information corresponding to the information code sequence other than the first redundant code and the second redundant code and a second soft-output code information corresponding to the second redundant code;

a plurality of soft-output buffers that store the first soft-output code information and the second redundant code;

an iterative detector that executes an error-correction to the first soft-output code information using the second soft-output code information, and outputs an error-correction decoded sequence; and

an error-correction demodulator that corrects a code error in the error-correction decoded sequence using the first redundant code.

~~each of plural error correction decoding circuits that detect and correct a code error using each error correction coding applied to each code sequence block~~

~~receives soft-output information for each code bit output from the soft-output decoder, receives soft-output information output from another error-correction decoding circuit, repeats the error detection and correction at plural times for each code sequence block and outputs the result of the error detection and correction as the result of the reproduction of the information code sequence after the error detection and correction are repeated by a predetermined frequency.~~

6. (Currently amended) The recording/reproducing signal processing circuit ~~An information recording/reproducing encoding circuit~~ according to claim 5, said iterative detector further comprising a parity decoder that executes said error-correction by updating the code bit of the first soft-output code information to more reliable code bit using the second soft-output code information.

~~comprising: a memory circuit that holds the contents of information data sector to which redundant codes are added by the first error-correction coding, which is a code sequence output from the encoding circuit that executes the first error-correction coding, an encoding permutation circuit that refers the contents of a code sequence in the information data sector, permutes them and outputs, an encoding circuit applies the second error-correction coding to the code sequence output from the encoding permutation circuit,a decoding circuit receives a reproduced signal sequence supplied from the recording medium in the detection and correction of a code error in the corresponding information data sector, receives soft-output information for each code bit acquired as a result of the code error detection and correction repeated by the second error-correction coding at a predetermined frequency, outputs the information of soft output decoding for each code bit again~~

~~and repeats the second error-correction coding using this information of soft-output decoding.~~

7. (Currently amended) The recording/reproducing signal processing circuit ~~An information recording/reproducing-encoding circuit~~ according to claim 5, wherein the error-correction by the iterative detector or the error-correction demodulator ~~:~~

~~the error-code-detection-and-correction by the first error-correction coding or the error-code-detection and correction of a code error by the second error-correction coding~~ is repeated only in case ~~in the error-code-detection-and-correction by the first error-correction coding,~~ code errors are detected and all the detected code errors cannot be corrected.

8. – 13. (Cancelled)

14. (Currently amended) An integrated circuit comprising a recording/reproducing signal processing circuit according to claim 3~~, wherein:~~

~~the information recording/reproducing-encoding circuit according to claim 3 is mounted~~.

15. (Currently amended) A magnetic hard disk drive apparatus comprising a recording/reproducing signal processing circuit according to claim 3~~, wherein:~~

~~the information recording/reproducing encoding circuit according to claim 3 or the integrated circuit according to claim 14 is mounted~~.